

## **ABSTRACT**

A CMOS inverter having a heterostructure including a Si substrate, a relaxed  $\text{Si}_{1-x}\text{Ge}_x$  layer on the Si substrate, and a strained surface layer on said relaxed  $\text{Si}_{1-x}\text{Ge}_x$  layer; and a pMOSFET and an nMOSFET, wherein the channel of said pMOSFET and the channel of the  
5 nMOSFET are formed in the strained surface layer. Another embodiment provides an integrated circuit having a heterostructure including a Si substrate, a relaxed  $\text{Si}_{1-x}\text{Ge}_x$  layer on the Si substrate, and a strained layer on the relaxed  $\text{Si}_{1-x}\text{Ge}_x$  layer; and a p transistor and an n transistor formed in the heterostructure, wherein the strained layer comprises the channel of the n transistor and the p transistor, and the n transistor and the p transistor are interconnected  
10 in a CMOS circuit.